For each step in the program below, indicate whether a register is being written to by entering a “W”, read from by entering an “R” or not involved by leaving it blank.

I1. LD r1, (r8)

I2. SUB r3, r5, r9

I3. XOR r7, r5, r1

I4. ST (r4), r2

I5. NOR r10, r12, r9

I6. AND r7, r6, r9

I7. NAND r5, r6, r2

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 | R12 |
| I1 |  |  |  |  |  |  |  |  |  |  |  |  |
| I2 |  |  |  |  |  |  |  |  |  |  |  |  |
| I3 |  |  |  |  |  |  |  |  |  |  |  |  |
| I4 |  |  |  |  |  |  |  |  |  |  |  |  |
| I5 |  |  |  |  |  |  |  |  |  |  |  |  |
| I6 |  |  |  |  |  |  |  |  |  |  |  |  |
| I7 |  |  |  |  |  |  |  |  |  |  |  |  |

Indicate any data dependencies and their type.

|  |  |  |  |
| --- | --- | --- | --- |
| **Register** | **Dependency** | **Instructions**  **Involved** | **Restriction** |
|  |  |  |  |
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Write the program, splitting it up for processing by as many different execution units as possible.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Pipeline 1** | **Pipeline 2** | **Pipeline 3** | **Pipeline 4** |
| **Time→** |  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |